ABSTRACT OF THE DISCLOSURE

A semiconductor device capable of achieving downsizing without reducing the power supply efficiency and capable of reducing switching noises and a memory card using the same are disclosed. The device comprises a plurality of stages of voltage booster circuits for potentially raising a power supply voltage up to a final output voltage, a voltage control unit for controlling an output voltage at a nearby location of the final stage, and one or more internal elements to which the final output voltage is supplied. A primary voltage booster circuit at the first stage includes an inductance element, a switching element, a diode and a driver circuit. At a metal core part of the inductance element, a metal wiring line is used, which was formed by use of a fabrication process of semiconductor integrated circuits, while employing for its core part an inter-wiring layer dielectric film that was formed using the fabrication process. In addition, the switching element and the diode are arranged so that portions thereof are disposed beneath the inductance element.

(12)特許協力条約に基づいて公開された国際出願

(19) 世界知的所有権機関
国際事務局

(43) 国際公開日
2004 年3 月25 日 (25.03.2004)

PCT

(10) 国際公開番号
WO 2004/025730 A1

(51) 国際特許分類[7]: H01L 27/04, H02M 3/155, G11C 17/00, H02M 3/00

(21) 国際出願番号: PCT/JP2003/010178

(22) 国際出願日: 2003 年8 月8 日 (08.08.2003)

(25) 国際出願の言語: 日本語

(26) 国際公開の言語: 日本語

(30) 優先権データ:
特願2002-233909 2002 年8 月9 日 (09.08.2002) JP
特願2002-274255 2002 年9 月20 日 (20.09.2002) JP

(71) 出願人 (米国を除く全ての指定国について): 株式会社日立製作所 (HITACHI, LTD.) [JP/JP]; 〒101-8010 東京都 千代田区 神田駿河台四丁目 6 番地 Tokyo (JP).

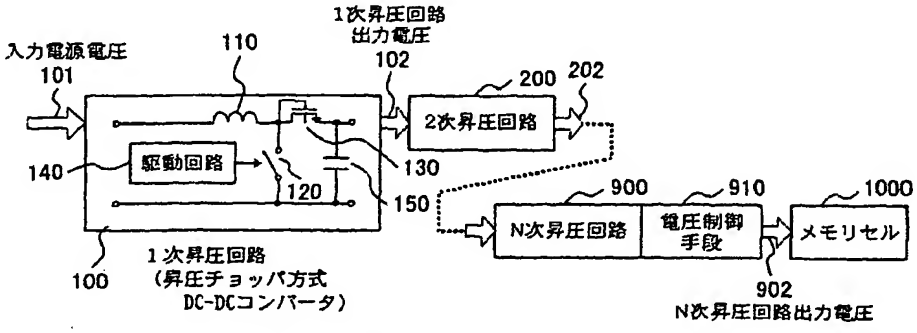
(72) 発明者; および

(75) 発明者/出願人 (米国についてのみ): 菊地 睦 (KIKUCHI,Mutsumi) [JP/JP]; 〒319-1292 茨城県 日立市 大みか町七丁目 1 番 1 号 株式会社日立製作所 日立研究所内 Ibaraki (JP). 秋山 登 (AKIYAMA,Noboru) [JP/JP]; 〒319-1292 茨城県 日立市 大みか町七丁目 1 番 1 号 株式会社日立製作所 日立研究所内 Ibaraki (JP). 庄司 浩幸 (SHOJI,Hiroyuki) [JP/JP]; 〒319-1292 茨城県 日立市 大みか町七丁目 1 番 1 号 株式会社日立製作所 日立研究所内 Ibaraki (JP). 村林 文夫 (MURABAYASHI,Fumio) [JP/JP]; 〒319-1292 茨城県 日立市 大みか町七丁目 1 番 1 号 株式会社日立製作所 日立研究所内 Ibaraki (JP). 叶田 玲彦 (KANOUDA,Akihiko) [JP/JP]; 〒319-1292 茨城県 日立市 大みか町七丁目 1 番 1 号 株式会社日立製作所 日立研究所内 Ibaraki (JP). 佐瀬 隆志 (SASE,Takashi)

[続葉有]

(54) Title: SEMICONDUCTOR DEVICE AND MEMORY CARD USING SAME

(54) 発明の名称: 半導体装置およびそれを用いたメモリカード



101...INPUT POWER SUPPLY VOLTAGE
140...DRIVE CIRCUIT
100...PRIMARY STEP-UP CIRCUIT (DC-DC CONVERTER OF STEP-UP CHOPPER TYPE)
102...PRIMARY STEP-UP CIRCUIT OUTPUT VOLTAGE
200...SECONDARY STEP-UP CIRCUIT
900...*N*-ARY STEP-UP CIRCUIT
910...VOLTAGE CONTROL MEANS
902...*N*-ARY STEP-UP CIRCUIT OUTPUT VOLTAGE
1000...MEMORY CELL

(57) Abstract: A semiconductor device that is small in size without marring the efficiency of the power supply and produces reduced noise in switching and a memory card are disclosed. The semiconductor device comprises step-up circuits connected into multistage for stepping up the power supply voltage to a predetermined final output voltage, a voltage control section for controlling the output voltage at the final stage or at a stage near the final stage, and an internal device to which the final output voltage is applied. The initial stage primary step-up circuit has an inductance element, a switching element, a diode, and a drive circuit. A metal coil section of the inductance element includes a metal wiring formed at the step of fabricating the semiconductor integrated circuit, and a core section includes an insulating film between wiring layers. The insulating film is formed at the same step of fabricating the semiconductor integrated circuit. The switching element and a part of the diode are disposed below the inductance element.

(57) 要約: 電源の効率を下げずに小型化が図れ、スイッチング時のノイズを低減できる半導体装置及びそれを用いたメモリカードであって、電源電圧を所定の最終

[続葉有]

WO 2004/025730 A1